A DUAL DIRECTION OVER-VOLTAGE AND OVER-CURRENT IC PROTECTION DEVICE AND ITS CELL STRUCTURE

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ABSTRACT

A two terminal ESD protection structure formed by an alternating arrangement of adjacent p-n-p-n-p semiconductor regions provides protection against both positive and negative ESD pulses. When an ESD pulse appears across the two terminals of the ESD protection structure, one of the inherent n-p-n-p thyristors is triggered into a snap-back mode thereby to form a low impedance path to discharge the ESD current.

Some embodiments of the ESD protection structure of the present invention have an enhanced current handling capability and are formed by combining a number of standard cells. The standard cells include a corner cell, a center cell and an edge cell which are arranged adjacent each other to form an ESD protection structure which provides for current flow from across many locations therein.

Some embodiments of the ESD protection structure of the present invention include a network consisting of a pair of current sources, e.g. back-to-back zener diodes, each connected in series with a resistor to control the trigger voltage of the ESD protection structure.